



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Cheng-Lien Chiang  
Assignee: Bridge Semiconductor Corporation  
Title: OPTOELECTRONIC SEMICONDUCTOR PACKAGE DEVICE  
Serial No.: 10/082,500 Filed: February 25, 2002  
Examiner: Chu, C. Group Art Unit: 2815  
Atty. Docket No.: BDG005-3

COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PETITION FOR WITHDRAWAL OF DRAWING OBJECTION  
FOR MISSING FEATURE IN CLAIMS 3, 11 AND 22**

Dear Sir:

This Petition is filed under 37 C.F.R. § 1.181 to request that the outstanding requirement to correct the drawings for a missing feature in claims 3, 11 and 22 under 37 C.F.R. § 1.83(a) be withdrawn.

**I. FACTS**

The captioned-application discloses an optoelectronic semiconductor package device and its method of manufacture.

The method includes providing semiconductor chip 110 that includes upper surface 112 and lower surface 114, where upper surface 112 includes light sensitive cell 115 and conductive pads 116 (Specification, page 8, lines 5-11 and Figs. 1A and 1B), providing metal base 120 that includes surfaces 122 and 124, central portion 126, slots 128, recessed portions 132 and 134,

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non-recessed portions 136 and leads 138 (Specification, page 9, lines 8-17 and Figs. 2A and 2B), forming metal traces 144 on metal base 120, where conductive traces 150 include leads 138 and metal traces 144 (Specification, page 11, lines 6-11 and Figs. 3A and 3B), forming transparent adhesive 154 on metal base 120 and metal traces 144 (Specification, page 12, lines 21-22 and Figs. 4A and 4B), mechanically attaching chip 110 to metal base 120 using transparent adhesive 154 (Specification, page 13, lines 5-6 and Figs. 5A and 5B), forming encapsulant 156 on chip 110 and metal base 120, where encapsulant 156 includes bottom surface 160, peripheral side surfaces 162, top surface 164 and peripheral portion 166 (Specification, page 14, lines 3-4 and page 14, line 30 to page 15, line 1 and Figs. 6A and 6B), removing encapsulant 156 from laterally extending portions of slots 128 (Specification, page 15, lines 22-23 and Figs. 7A and 7B), forming protective coating 170 on metal base 120 outside encapsulant 156 (Specification, page 16, lines 9-10 and Figs. 8A and 8B), removing central portion 126 of metal base 120, thereby exposing metal traces 144 and transparent adhesive 154 (Specification, page 17, lines 7-8 and 12-13 and Figs. 9A and 9B), forming openings 176 in transparent adhesive 154 that expose pads 116 (Specification, page 18, lines 7-9 and Figs. 10A and 10B), forming connection joints 180 in openings 176 that contact and electrically connect pads 116 and metal traces 144 (Specification, page 18, line 28 to page 19, line 2 and Figs. 11A and 11B), forming transparent base 182 on the structure, where encapsulant 156 and transparent base 182 in combination form insulative housing 184 that surrounds and encapsulates chip 110 (Specification, page 20, lines 3-4 and 20-21 and Figs. 12A and 12B), singulating optoelectronic device 186 from the lead frame (Specification, page 21, lines 1-2 and 6-7 and Figs. 13A and 13B), and bending leads 138 (Specification, page 21, lines 18-20 and Figs. 14A and 14B).

Claim 3 recites “the first housing portion is spaced from the upper surface [of the chip].” Claims 11 and 22 recite similar limitations.

The Office Action dated April 10, 2003 objects to the drawings under 37 C.F.R. § 1.83(a) since the limitation in claims 3, 11 and 22 “the first housing portion is spaced from the upper surface” is not shown in the drawings.

The Response dated April 24, 2003 requested that the objection be withdrawn.

The Office Action dated July 31, 2003 maintained the objection, includes a reproduction of Fig. 6C with the corner between upper surface 112 of chip 110 and the left outer side surface of chip 110 labeled as the area "A" and states as follows:

As shown in the above Fig. 6C, the area "A" clearly shows that the encapsulant 156 contacts the surface 112 of chip 110, not spaced from the surface 112 of the chip 110.

## II. ARGUMENT

The upper surface is illustrated as surface 112 of chip 110 in Fig. 1B, and the first housing portion is illustrated as encapsulant 156 in Figs. 6A to 6D. Surface 112 of chip 110 contacts and is covered by transparent adhesive 154 in Fig. 5A. As a result, encapsulant 156 is spaced from surface 112 of chip 110, as shown in Figs. 6C, 6D, 7C, 7D, 9B, 10B, 11B, 12B, 12C, 13B and 14B.

Furthermore, transparent adhesive 154 is deposited as a liquid resin on metal base 120 and metal traces 144 (Specification, page 12, lines 22-25). The liquid resin is compliant enough at room temperature to conform to virtually any shape (Specification, page 12, lines 28-29). Transparent adhesive 154 is then sandwiched between chip 110 and metal base 120 using relatively low pressure (Specification, page 13, lines 21-22). Thereafter, transparent adhesive 154 is heated and fully cured at relatively low temperature of about 150°C to form a solid adhesive transparent electrically insulative die attach that mechanically fastens chip 110 to metal base 120 and metal traces 144 (Specification, page 13, lines 22-24).

The Examiner asserts that encapsulant 156 contacts surface 112 of chip 110 in Fig. 6C. This is clearly erroneous. Transparent adhesive 154 contacts the entire surface 112 of chip 110 and encapsulant 156 is spaced from surface 112 of chip 110 in Fig. 6C.

The Examiner also asserts that *Nakamura et al.* (U.S. Patent No. 5,405,809) discloses that resin coating 27 is spaced from the upper surface of image sensor chip 26 in Fig. 2 to reject claims 3, 11 and 22. Resin coating 27 is shown adjacent to the lower left corner of image sensor chip 26 in Fig. 2 of *Nakamura et al.* exactly as encapsulant 156 is shown adjacent to the lower left corner of chip 110 in Fig. 6C of the captioned-application. In other words, the area “A” labeled in Fig. 6C of the captioned-application also arises in Fig. 2 of *Nakamura et al.*

Thus, the Examiner asserts that the encapsulant contacts the upper surface of the chip at the area “A” for the purpose of objecting to the drawings as not showing the features in claims 3, 11 and 22, but on the other hand, asserts that the encapsulant is spaced from the upper surface of the chip at the area “A” for the purpose of rejecting claims 3, 11 and 22 over *Nakamura et al.*

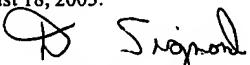
The Examiner’s positions contradict one another and it is improper and unfair for the Examiner to adopt this tactic.

Finally, even though encapsulant 156 is shown near upper surface 112 of chip 110 in Fig. 6C, since chip 110 contacts transparent adhesive 154 using relatively low pressure while transparent adhesive 154 is a liquid resin, and then transparent adhesive 154 is fully cured to form a solid adhesive die attach, those skilled in the art would understand that in Fig. 6C, transparent adhesive 154 would contact the outer side surface of chip 110 at the corner with upper surface 112 of chip 110, thereby preventing encapsulant 156 from contacting upper surface 112 of chip 110. Die attach materials are often shown as not contacting the outer side surface of the chip to simplify the drawings by omitting a relatively unimportant detail. See, for instance, *Nakamura et al.*, as well as *Fjelstad* (U.S. Patent No. 6,001,671) and *Tsuji et al.* (U.S. Patent No. 6,025,650), all cited by the Examiner.

Therefore, Applicant requests that this objection be withdrawn.

Please charge any fee due under this Petition to Deposit Account No. 502178/BDG005-3.

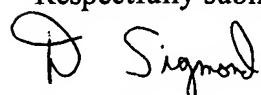
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 18, 2003.



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Respectfully submitted,



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